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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,670	11/18/2003	Sungkwon C. Hong	M4065.0982/P982	2308

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,670	HONG, SUNGKWON C.	
	Examiner	Art Unit	
	Thinh T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-21 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-12 and 46* is/are allowed.

6)☒ Claim(s) *13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 9-21 and 46 are pending in the application.

2. New found references necessitate new ground of rejection for some claims in the application; therefore, the Office Action issued on 2/10/2006 is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 13-15 , 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Blair et al. (U.S. Patent 6,171,901).

REGARDING CLAIM 13

Blair discloses (in fig 3L, in column 5 lines 63-67, column 6 lines 1-9) a method of forming a memory cell, comprising the steps of: forming a transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in the semiconductor substrate disposed adjacent to the gate, the step of forming the transistor including providing a silicide region of the gate; and forming a capacitor adjacent the transistor by providing a first conductive

layer, a dielectric layer and a second conductive layer, wherein the steps of providing the first conductive layer, the dielectric layer and the second conductive layer are conducted prior to the step of providing the silicide region of the gate.

Noted that in the rejection of claim 13, the preamble is not given any patentable weight. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

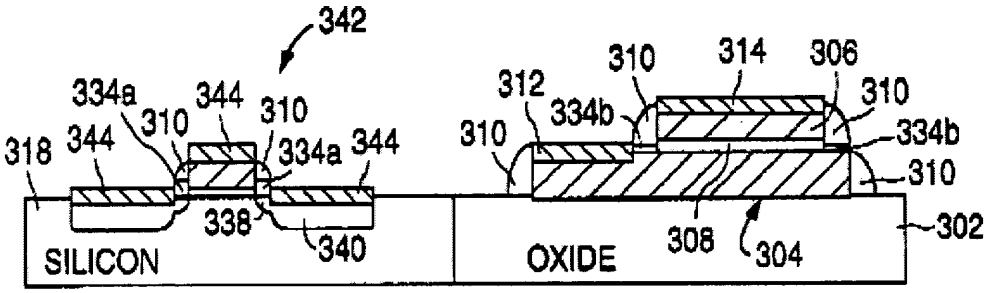

FIG. 3L

REGARDING CLAIM 14

Blair discloses (in fig 3C, in column 4 lines 49-51) a method wherein the first conductive layer is formed of doped polysilicon.

REGARDING CLAIM 15

Blair discloses (in fig 3B, in column 4 lines 38-44) a method wherein the second conductive layer is formed of doped polysilicon.

REGARDING CLAIM 17

Blair discloses (in claim 19, the last step) a method wherein the step of providing the silicide region of the gate includes providing a metal layer a gate electrode and annealing the metal layer to form the silicide layer.

REGARDING CLAIM 18

Blair discloses (in fig 3L, in column 6 line 1) a CMOS FET transistor and CMOS (Complementary Metal Oxide) is inherently a MOSFET transistor.

REGARDING CLAIM 19

Blair discloses (in fig 3A) a method wherein the substrate is silicon.

Claim Rejections - 35 USC § 103

5. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blair et al. (US patent 6,171,901).

REGARDING CLAIM 16

With regard to claim 16, as set forth in the rejection of claim 13, Blair discloses all the invention except for the condition that the second conductive layer is formed by deposition at a temperature between about 600 degree to 800 degree Celsius.

It would have been obvious to one of ordinary skill in the art the time the invention was made to set the deposition temperature of second conductive layer at a temperature between about 600 degree to 800 degree Celsius in the Blair method since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

7. Claim 20, 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blair et al. (US patent 6,171,901) in view of Crafts (US patent 5,973,952)

REGARDING CLAIM 20-21

With regard to claim 20,21 as set forth in the rejection of claim 13, Blair discloses all the invention except for the condition that the memory cell is a DRAM. Crafts, however, (in fig 3, in the abstract) discloses a method to make DRAM in semiconductor device. it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of making DRAM cell disclosed by Crafts into the method by Blair since both the two inventions are in the same field of endeavor of making mixed signal devices (see Blair reference column 1 line 15 and Craft reference column 1 line 7-8).

ALLOWABLE SUBJECT MATTER

8. Claims 9-12, 46 are allowable

Claim 9-12, 46 are considered allowable since the prior fails to show a method for forming a memory devices with the steps:

-- " forming at least one in-pixel gate structure in an array region of a substrate, the at least one in-pixel gate structure being further formed by providing a first doped conductive layer over the substrate and providing a first silicide region over the first doped conductive layer; "--

and

-- " forming at least one capacitor structure over an isolation region in the array region, the at least one capacitor structure being further formed by providing a first capacitor electrode layer, providing a dielectric layer over the first capacitor electrode layer, and providing a second capacitor electrode layer over the dielectric layer, wherein the steps of providing the first and second silicide regions are conducted subsequent to the step of providing the second capacitor electrode layer."--

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three)

months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T. Nguyen TTN
Art Unit 2818

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Technology Center 2800